**IN THE CLAIMS:**

Please cancel claims 4-7, 10, 11, and 34 without prejudice or disclaimer as to the subject matter contained therein.

Please amend the claims as shown in the following claims listing.

1. (Currently amended) A system, comprising:

a node including a processing subsystem and an interface coupled by an address network and a data network;

an additional node including an additional processing subsystem and an additional interface coupled by an additional address network and an additional data network;

an inter-node network configured to convey communications between the node and the additional node, wherein the interface and the additional interface are coupled to send and receive communications on the inter-node network;

wherein as part of a coherency transaction involving a coherency unit cached by the processing subsystem, the processing subsystem is configured to transition an access right to the coherency unit in response to the processing subsystem receiving a data packet via the data network, and to transition an ownership responsibility for the coherency unit in response to receiving [[an]] a corresponding address packet on the address network, wherein the processing subsystem transitions the access right at a different time than the processing subsystem transitions the ownership responsibility;

wherein the address packet and the data packet are part of a read-to-own transaction initiated by the processing subsystem; [[and]]

wherein the interface in the node is configured to delay providing the data packet on the data network until the interface receives an indication that shared copies of the coherency unit in the additional node have been invalidated;

wherein in response to receiving the address packet via the address network, a memory subsystem included in the node is configured to send a data packet indicating the read-to-own transaction to the interface, wherein the interface is configured to forward a read-to-own message on the inter-node network in response to receiving the data packet indicating the read-to-own transaction; and

wherein the additional interface is configured to receive the read-to-own message via the inter-node network and to responsively send an invalidating address packet on the additional address network, wherein in response to the additional processing subsystem having an access right to but not an ownership responsibility for the coherency unit, the additional processing subsystem is configured to transition its access right to the coherency unit in response to the invalidating address packet.

2-7. (Cancelled)

8. (Currently amended) The system of claim [[7]] 1, wherein the interface is configured to forward a read-to-own message corresponding to the address packet to the additional interface via the inter-node network in response to receiving the address packet.

9. (Original) The system of claim 8, wherein the coherency unit is not mapped by any memory subsystem included in the node, and wherein the additional node is a home node for the coherency unit.

10-11. (Cancelled)

12. (Original) The system of claim 11, wherein in response to receiving the invalidating address packet on the additional address network, the additional interface is configured to send via the inter-node network a message indicating that copies of the coherency unit in the additional node have been invalidated to the interface.

13. (Previously presented) The system of claim 12, wherein the additional interface is configured to send an additional address packet on the additional address network, wherein if the additional processing subsystem has an ownership responsibility associated with the coherency unit, the additional processing subsystem is configured to transition the ownership responsibility to the coherency unit upon receiving the additional address packet.

14. (Original) The system of claim 13, wherein the additional processing subsystem is configured to send a data packet corresponding to the coherency unit to the additional interface in response to receiving the additional address packet, wherein the additional processing subsystem is configured to transition an access right associated with the coherency unit in response to sending the data packet corresponding to the coherency unit.

15-16. (Cancelled)

17. (Original) The system of claim 1, wherein the access right to the coherency unit cached by the processing subsystem transitions in response to the processing subsystem receiving a data packet via the data network, wherein the data packet is provided to the processing subsystem as part of a write stream transaction initiated by the processing subsystem.

18. (Original) The system of claim 17, wherein the data packet is an encoded acknowledgment that excludes data corresponding to the coherency unit.

19. (Currently amended) A system, comprising:

a node including a processing subsystem and an interface coupled by an address network and a data network;

an additional node including an additional processing subsystem and an additional interface coupled by an additional address network and an additional data network;

an inter-node network configured to convey communications between the node and the additional node, wherein the interface and the additional interface are coupled to send and receive communications on the inter-node network;

wherein the processing subsystem is configured to transition an access right to a coherency unit in response to a data packet on the data network and to transition an ownership responsibility for the coherency unit in response to receiving [[an]] a corresponding address packet on the address network;

wherein the address packet and the data packet are part of a read-to-own transaction initiated by the processing subsystem; [[and]]

wherein the interface within the node is configured to delay providing the data packet on the data network until the interface receives an indication from the additional interface via the inter-node network that any shared copies of the coherency unit in the additional node have been invalidated;

wherein in response to receiving the address packet via the address network, a memory subsystem included in the node is configured to send a data packet indicating the read-to-own transaction to the interface, wherein the interface is configured to forward a read-to-own message on the inter-node network in response to receiving the data packet indicating the read-to-own transaction; and

wherein the additional interface is configured to receive the read-to-own message via the inter-node network and to responsively send an invalidating address packet on the additional address network, wherein in response to the additional processing subsystem having an access right to but not an ownership responsibility for the coherency unit, the additional processing subsystem is configured to transition its access right to the coherency unit in response to the invalidating address packet.

20. (Previously presented) The system of claim 19, wherein the transaction also includes an additional address packet sent on the additional address network and at least one message sent on the inter-node network.

21. (Cancelled)

22. (Previously presented) The system of claim 20, wherein the additional interface is configured to broadcast an invalidating address packet on the additional address network in response to receiving a message indicating the transaction from the interface via the inter-node network.

23. (Previously presented) The system of claim 20, wherein the additional interface is configured to send an acknowledging message to the interface via the inter-node network in response to the additional interface receiving the invalidating address packet on the additional address network, wherein the acknowledging message includes the indication that shared copies of the coherency unit in the additional node have been invalidated;

wherein if the additional processing subsystem has an access right to but not ownership of the coherency unit, the additional processing subsystem is configured to transition the access right to the coherency unit upon receipt of the invalidating address packet.

24. (Original) The system of claim 20, wherein the transaction is a read-to-own transaction, wherein the processing subsystem is configured to initiate the read-to-own transaction by sending a read-to-own packet on the address network.

25. (Original) The system of claim 24, wherein no memory subsystem included in the node maps the coherency unit;

wherein in response to the read-to-own packet on the address network, the interface is configured to send a read-to-own message to the additional interface in the additional node.

26. (Original) The system of claim 19, wherein the address network is configured to convey the address packet from a directory to the processing subsystem in point-to-point mode.

27. (Original) The system of claim 19, wherein the address network is configured to convey the address packet in broadcast mode.

28-34 (Cancelled)